IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Yeo, *et al.*	Attorney Docket:	TSM03-0421
Filed:	June 27, 2003	Examiner:	TBD
Serial No.:	10/608,287	Art Unit:	2812

For: Structure and Method for Forming the Gate Electrode in a Multiple-Gate Transistor

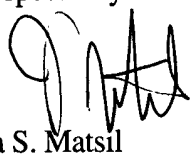
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO-1449 that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed pursuant to 37 C.F.R. § 1.97(b)(3), before the mailing of a first Office action on the merits.

Respectfully submitted,



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PTO/SB/08A (02-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known	
Application Number	10/608,287
Filing Date	June 27, 2003
First Named Inventor	Yeo, *et al.*
Art Unit	2812
Examiner Name	TBD
Attorney Docket Number	TSM03-0421

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number - Kind Code[2] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A	US-6,252,284 B1	06-26-2001	Muller, *et al.*	
	B	US-6,391,695 B1	05-21-2002	Yu	
	C	US-6,391,782 B1	05-21-2002	Yu	
	D	US-6,413,802 B1	07-02-2002	Hu, *et al.*	
	E	US-6,432,829 B2	08-13-2002	Muller, *et al.*	
	F	US-6,451,656 B1	09-17-2002	Yu, *et al.*	
	G	US-6,492,212 B1	12-10-2002	Ieong, *et al.*	
	H	US-2003/0067017 A1	04-10-2003	Ieong, *et al.*	
	I	US-2003-0102497 A1	06-05-2003	Fried, *et al.*	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] - Number[4] - Kind Code[5] (*if known*)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet	2	of	2

Compl te if Known	
Application Number	10/608,287
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Group Art Unit	2812
Examiner Name	TBD
Attorney Docket Number	TSM03-0421

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	J	HUANG, X., *et al.* "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5 (May 2001) pp. 880-886.	
	K	YANG, F-.L., *et al.* "35nm CMOS FinFETs," 2002 Symposium on VLSI Technology Digest of Technical Papers, (June 2002) pp. 109-110.	
	J	WONG, H-.S.P. "Beyond the Conventional Transistor," IBM Journal of Research and Development, Vol. 46, No. 2/3 (March/May 2002) pp. 133-167.	
	L	CHAU, R., *et al.* "Advanced Depleted-Substrate Transistors: Single-gate, Double-Gate and Tri-Gate," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, (2002) pp. 68-69.	
	M	YANG, F-.L., *et al.* "25nm CMOS Omega FETs," International Electron Devices Meeting, Digest of Technical Papers, (December 2002) pp. 255-258.	
	N	COLINGE, J.P., *et al.* "Silicon-On-Insulator 'Gate -All-Around Device," International Electron Devices Meeting, (1990) pp. 595-598.	
	O	LEOBANDUNG, E., *et al.*, "Wire-Channel and Wrap-Around-Gate Metal-Oxide-Semiconductor Field-Effect Transistors with a Significant Reduction of Short Channel Effects," Journal of Vacuum Science and Technology, Vol. B 15, No. 6, (November/December 1997) pp. 2791-2794.	

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